



**BHARATI VIDYAPEETH UNIVERSITY,
Pune.**

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COURSE STRUCTURE & SYLLABUS
M. Tech (Electronics) (Semester - I to IV)



COURSE STRUCTURE & SYLLABUS

BHARATI VIDYAPEETH UNIVERSITY, PUNE

M. Tech. (ELECTRONICS-VLSI) (Sem. I to IV)



HIGHLIGHTS

Bharati Vidyapeeth University College of Engineering (BVUCOE) is the largest Engineering College in Maharashtra with an intake of 700 students in each academic year. Imparting quality technical education from Under Graduate to Doctorate Level, BVUCOE is probably the only Engineering College in India with an accreditation from both NAAC as well as NBA. The faculty at BVUCOE boasts of highly qualified academicians, a quality that is further emphasized by the fact that 15 of them are presently pursuing their Ph.D. degree.

BVUCOE has been ranked 29th amongst the Top 50 Technical Schools of India in survey conducted by DATAQUEST-IDC. We have enjoyed a ranking in this list for the last 4 years. Research is of utmost importance in all our programs. A total of 113 research papers were published in the academic year 2007-2008.

Currently we have 12 ongoing research projects. The infrastructure of BVUCOE is state-of-the-art with 62 classrooms, 59 laboratories and a well-stocked library that currently holds 27,130 titles. The college has an international presence with MoUs signed with the North Carolina A&T State University (Greensboro, USA), University of Venice (Italy), Actel Corporation (USA). Corporate interaction is also inculcated in our programs through our association with Oracle India Ltd., Infosys Ltd. and Tata Consultancy Services.

SALIENT FEATURES

India is the fourth largest telecom market in Asia. The Indian telecom market is eighth largest in the world and second largest among emerging economies. The industry has witnessed an explosive growth in the field of electronics in the recent years. India has institutions that are deeply rooted in the principles of democracy and Justice. This ensures a transparent, predictable and secure environment for development of electronics field.

The National Telecom policy 1999 (NT 99) targets tele-density at 15 per cent by 2010. The Indian market presents a unique opportunity as compared to developed countries, hence increasing the attractiveness of the Indian market.

In the engineering field, electronics branch is one of the most significant as it reflects today's changing technology. It has become a must-know field as it forms the base for all other engineering branches.

To comply with the present day requirements & keep pace with the recent technology, the course is designed to provide the students with technical know-how. The department therefore aims to ensure that the students excel in hardware as well as software technologies. The department has started post-graduate course leading to M.E. Electronics (VLSI) which focuses on the theory, design, implementation and application of this upcoming technology in technical context.

The department has received a grant of Rs. 45.5 Lakhs from UGC under their innovative program scheme to start the Biomedical Engineering course with the intake capacity of 40 students.

College has established collaboration with ACTEL Corporation, USA. Under this collaboration an advanced VLSI laboratory is established jointly. For this laboratory, ACTEL Corporation has provided software and hardware worth \$3, 56,000 (Approx. 1.5 Crores)

The department has well-qualified and experienced staff with 6 Professors, 2 Assistant-Professors and 11 lecturers. Most of them have completed post-graduation and some are pursuing.

MAJOR GROUPS / AREAS

Image Processing, Digital Signal Processing, Very Large Scale Integration, Biomedical Engineering, Fiber optic sensors

EXPERTISE IN RESEARCH AND CONSULTANCY

Electronics engineering department received a grant of 6.5 lakhs from All India Council for Technical Education (AICTE), New Delhi for development of DSP laboratory under MODROB scheme. Research has been carried out in the field of signal

processing, control and communication with credit of five research papers published at national level. Three staff members are pursuing PhD work in the field of signal processing and communication. The department has received the grant of Rs. 70, 000 from Institute of Engineers, Pune for various research projects undertaken by students.

MAJOR EQUIPMENT

Mixed Signal Oscilloscope, Vector Voltmeter, Digital Storage Oscilloscope, Wobbuloscope, Powerscope, Allen-Bradley PLC with RSLogix500 software, Ratio Control Unit Trainer, ICAP 4, DSP Processor Training Boards & EVMs, X-ray machine (Demo type), Ultrasound scanner (Demo type), Blood cell counter, EEG hardware and software, Spectrophotometer (Demo type), Gas chromatography system (Demo type), ECG stress test software with thread mill

SOFTWARE

ORCAD, XI LINX 3.1, Altera, MATLAB, LabView, ALDEC, Code Composer Studio, Libero

LABORATORIES

ACTEL-VLSI Lab, Microelectronics Laboratory, Digital Electronics Laboratory, Network and Lines Laboratory, Electric Circuit Design and Project Laboratory, Communication Laboratory, Microprocessor and Microcontroller Laboratory, Computer Networking Laboratory, DSP and Image Processing Laboratory, Electronic Instrumentation and Measurements, Power Electronics Laboratory, Instrumentation and Control Laboratory, Biomedical Laboratory, Computer Lab



STRUCTURE & EXAMINATION PATTERN

M. Tech. - (Electronics - VLSI)

| Semester I | | | | | | | | Total Duration : 20 Hrs/Week |
|-------------------|-------------------------------|------------------------|----|----------------------------|-----------|----|------|-------------------------------------|
| | | | | | | | | Total Marks : 500 |
| Subject Code | Subject | Teaching Scheme (Hrs.) | | Examination Scheme (Marks) | | | | Total (Marks) |
| | | L | P | Theory | Unit Test | TW | Oral | |
| K50501 | Microelectronics | 04 | - | 70 | 30 | - | - | 100 |
| K50502 | Embedded Systems | 04 | 02 | 70 | 30 | 25 | 25 | 150 |
| K50503 | Digital Communication Systems | 04 | 02 | 70 | 30 | 25 | 25 | 150 |
| K50504 | Discrete Mathematics | 04 | - | 70 | 30 | - | - | 100 |
| | Total | 16 | 04 | 280 | 120 | 50 | 50 | 500 |

| Semester II | | | | | | | | Total Duration : 20 Hrs/Week |
|--------------------|----------------------------|-----------------------------|----|----------------------------|-----------|----|------|-------------------------------------|
| | | | | | | | | Total Marks : 500 |
| Subject Code | Subject | Teaching Scheme (Hrs./week) | | Examination Scheme (Marks) | | | | Total (Marks) |
| | | L | P | Theory | Unit Test | TW | Oral | |
| K50505 | DSP based Design Systems | 04 | - | 70 | 30 | - | - | 100 |
| K50506 | VLSI for wireless networks | 04 | - | 70 | 30 | - | - | 100 |
| K50507 | VLSI Design | 04 | 02 | 70 | 30 | 25 | 25 | 150 |
| K50508 | System Simulation | 04 | 02 | 70 | 30 | 25 | 25 | 150 |
| | Total | 16 | 04 | 280 | 120 | 50 | 50 | 500 |

For M.Sc. Students only:

| | | | | | | | | | |
|---------|------------------------|----|----|----|----|---|---|---|-----|
| *K50405 | VLSI Design Technology | 04 | 02 | 30 | 70 | - | - | - | 100 |
| *K50306 | Embedded | 04 | 02 | 30 | 70 | - | - | - | 100 |

* These subjects are from UG/B.Tech. (Electronics) course.



STRUCTURE & EXAMINATION PATTERN

M. Tech. - (Electronics-VLSI)

| Semester III | | Total Duration : 15 Hrs/Week | | | | | | |
|---------------------|----------------------|-------------------------------------|-----------|----------------------------|-----------|------------|-----------|---------------|
| Subject Code | Subject | Teaching Scheme Hrs/Week | | Examination Scheme (Marks) | | | | Total (Marks) |
| | | L | P | Theory | Unit Test | TW | Oral | |
| K50611 | Elective I | 04 | 02 | 70 | 30 | 25 | 25 | 150 |
| K50612 | Elective II | 04 | 02 | 70 | 30 | 25 | 25 | 150 |
| K50613 | Seminar | - | - | - | - | 25 | 25 | 50 |
| K50614 | Dissertation Stage I | - | 02 | - | - | 25 | - | 25 |
| | Total | 10 | 06 | 140 | 60 | 100 | 75 | 375 |

| Semester IV | | Total Duration : 15 Hrs/Week | | | | | | |
|--------------------|-----------------------|-------------------------------------|-----------|----------------------------|-----------|------------|-----------|---------------|
| Subject Code | Subject | Teaching Scheme Hrs/Week | | Examination Scheme (Marks) | | | | Total (Marks) |
| | | L | P | Theory | Unit Test | TW | Oral | |
| K50615 | Dissertation Stage II | - | 04 | - | - | 150 | 75 | 225 |
| | Total | - | 04 | - | - | 150 | 75 | 225 |

Elective - I

- Testing & Verification of VLSI Design
- Software Defined Radios
- Real Time System Design

Dissertation-I:

Problem Identification
Information Gathering
Literature Survey
Synopsis
System Analysis and Requirement Analysis
Plan of dissertation stage-II
Report of dissertation stage-I

Note:

- 6/7 students per batch for all practicals.
- One student per batch for seminar and project dissertation.
- For calculation of work load of the faculty the number of hours allocated to seminar and dissertation should be considered.
- The students should submit the Dissertation-I report along with the Dissertation-II(Final) Report.

Elective II

- Wireless Sensor Networks
- Algorithm for VLSI Design Automation
- Fuzzy Logic for Embedded System Application

Dissertation-II:

Building & Testing
System Documentation and Project Report
Publish at least on National/International report
Report of Dissertation Stage-II



RULES FOR CONDUCTING TESTS

Mode of the test

- Three unit tests per subject shall be conducted in each semester. The schedule for the same will be declared in the academic calendar of each term.
- Each unit test shall carry 30 marks.
- University examination pattern has given weightage of 30 marks for unit tests and 70 marks for theory examination
- To calculate final marks of the unit test following procedure is followed:
 - i) Out of the three unit tests conducted during the semester, the marks of only two unit tests in which the candidate has shown his/her best performance shall be considered, to decide the provisional marks in each subject
 - ii) Average marks obtained in two unit tests in which students have performed well shall be considered as provisional marks obtained by the student.
 - iii) If the candidate appears only for two unit tests conducted during the semester, he/she will not be given the benefit of the best performance in the tests.
 - iv) If the candidate appears only for one unit test conducted during the semester, to calculate the marks obtained in the unit tests it will be considered that the candidate has got 0(zero) marks in other unit tests.
 - v) There is separate passing in theory examination. A candidate has to secure minimum 28 marks(i.e.40%) out of 70 marks to declare him/her pass. Provisional marks obtained by the candidate in unit tests should reflect as proportional to the marks obtained in theory examination. In case of disparity of more than 15% it will be scaled down accordingly. These marks will be final marks obtained by the student. No scaling up is permitted.
 - vi) Unit test marks will be added in theory examination marks only after passing of candidate in theory examination in respective subject.
- Paper pattern for the unit tests:
- All questions are compulsory with weightage as following:

| | | |
|------------|---|----------|
| Question 1 | - | 10 marks |
| Question 2 | - | 10 marks |
| Question 3 | - | 10 marks |
- For granting the term it is mandatory to appear for all the three unit tests conducted in each semester.
- Roll numbers allotted to the students shall be the examination numbers for the unit tests.



SEMESTER - I



**TEACHING SCHEME**

Lectures : 04 Hrs/week

EXAMINATION SCHEME

Theory : 70 Marks

Duration : 03 Hours

Unit Test : 30 Marks

Unit-I

(08Hours)

Device Modelling:

Practical consideration in designing IC's size, complexity. IC fabrication process, trends in VLSI design. IC fabrication, packaging and testing, layout techniques and process parameters. DC models, small signal models of various components.

Unit-II

(08Hours)

MOS Technology and Circuits :

MOS Technology and VLSI, Process parameters and considerations for BJT, MOS and CMOS, Electrical properties of MOS circuits and Device modelling. MOS Transistors, MOS transistor switches.

Unit-III

(08Hours)

MOS Circuit Design Process :

MOS Layers, Stick Diagram, Layout diagram, Propagation delays, Examples of combinational logic design, Scaling of MOS circuits.

Unit-IV

(08Hours)

CMOS Circuits & Processing Technology:

CMOS Logic, Circuit and system representations (behavioral, structural, physical) CMOS Chip design. Basic CMOS Technology, CMOS process enhancements. Layout design rules. Technology related CAD issues.

Unit-V

(08Hours)

Circuit Characterization and Performance Estimation :

Estimation of resistance , capacitance, inductance, delays , CMOS – Gate transistor sizing, Power dissipation, Sizing, routing of conductors, Design margining, Yield, Reliability.

Unit-VI

(08Hours)

CMOS Circuits and Logic Design:

CMOS logic gate design, physical design of simple logic gates, CMOS logic structures, Clocking strategies, I / O structures, Low power design., Thin film and thick film technology, Introduction to nano technology

Text Books/ References

- Neil H. E. Weste, Kamran Eshraghian, "Principles of CMOS VLSI design", Pearson Education 2001
- Geiger, Allen Strader, "VLSI Design Techniques for Analog and Digital circuits", PHI
- Douglas A. Pucknell, Kamran Eshraghian, "Basis VLSI Design", PHI 2004.

Syllabus for Unit Test

| | |
|-------------|---------------|
| Unit Test 1 | Unit I & II |
| Unit Test 2 | Unit III & IV |
| Unit Test 3 | Unit V & VI |



TEACHING SCHEME

Lectures : 04 Hrs/week
Practical : 02 Hrs/week

EXAMINATION SCHEME

Theory : 70 Marks
Duration : 03 Hours
Unit Test : 30 Marks
T. W. : 25 Marks
Oral : 25 Marks

Unit-I

(08 Hours)

Introduction to Embedded Systems:

An Embedded system, Processor in Embedded Systems, Other hardware units, Software embedded into a system, embedded system on chip (SOC) and VLSI circuits.

Unit-II

(08 Hours)

Processor and Memory Organisation:

Structural units in processor, Processor selection for embedded system, memory devices, memory selection for an embedded system, allocation of memory, direct memory access, Interfacing Processors, Memories and I/O devices.

Unit-III

(10 Hours)

Devices and Buses for Device Networks:

I/O devices, timer and counting devices, serial communication, parallel communication.

Device Drivers and Interrupt Servicing Mechanism:

Device drivers, Parallel port device drivers, serial port device drivers, device drivers for internal programmable timing devices, interrupt servicing mechanism, context and the periods of context switching, deadline and interrupt latency.

Unit-IV

(08 Hours)

Program Modelling Concepts in Single and Multiprocessor Systems:

Software development process, modeling process for software analysis, Programming model for event control or response time, real time programs, modelling of multiprocessor systems.

Software Engineering Practices in the Embedded Software Development Process:

Software Algorithmic complexity, Software development process life cycle and its models, software analysis, software design, software implementation, software testing validating and debugging, real time programming issues, software project management, software maintenance, UML.

Unit-V

(08 Hours)

Interprocess Communication and Synchronization of Processes, Tasks and Threats:

Multiple processes in an application, Problem of sharing data by multiple tasks and routines, interprocess communication.

Real Time Operating System:

Operating system services, I/O subsystems, network operating system, real time and embedded operating system, interrupt routines in RTOS environment, RTOS task scheduling model, Interrupt latency & response time, performance metric in scheduling models, function of POSIX, Embedded Linux OS security issues, Mobile OS, study of $\mu\text{C}/\text{OS-II}$.

Unit-VI

(06 Hours)

Hardware Software Co-Design in Embedded System:

Embedded System project management, ES design and co-design issues in system development process design cycle.

List of Practical

- Minimum of one assignment on each topic should be conducted.

Text Books/References

- Rajkamal, "Embedded System-Architecture, programming and design", TMH Publication, edition 2003

Syllabus for Unit Test

| | |
|-------------|---------------|
| Unit Test 1 | Unit I & II |
| Unit Test 2 | Unit III & IV |
| Unit Test 3 | Unit V & VI |

**TEACHING SCHEME**

Lectures : 04 Hrs/week
Practicals : 02 Hrs/week

EXAMINATION SCHEME

Theory : 70 Marks
Duration : 03 Hours
Unit Test : 30 Marks
T. W. : 25 Marks
Oral : 25 Marks

Unit-I**(08 Hours)****Sampling & Pulse Modulation:**

Sampling of analog signals, sampling theorem in time and frequency domain, Nyquist rate, ideal, natural and flat top sampling, reconstruction of sampled signal by interpolation filter. PAM - TDM, cross-talk, guard time, ISI.

Unit-II**(08 Hours)****Information Theory:**

Discrete messages, Amount of Information, Average Information (Entropy), Information rate, Source coding, Shannon-Fano algorithm Huffman coding, Shannon's theorem, channel capacity of a Gaussian channel.

Unit-III**(08 Hours)****Digital Pulse Modulation:**

Block diagram of PCM transmitter and receiver, quantizing, encoding, quantization noise, non-uniform quantizing, μ law companding. PCM -TDM bit rate calculation, V90, 56 kb/s PCM computer mode. Digital multiplexing-(synchronous, asynchronous and quasi- synchronous). Differential PCM, Delta modulation Adaptive Delta modulation, vocoders, channel vocoder, linear predictive coder, line codes.

Unit-IV**(08 Hours)****Synchronization & Modulation Techniques:**

Bit synchronization, frame synchronization, scramblers & unscramblers, FEC, ARQ, performance of ARQ . Binary phase -shift keying, Differential PSK, Differential encoded PSK, Quadrature PSK, M-ary PSK, Quadrature

Amplitude shift keying Binary, Frequency shift-keying, M-ary FSK minimum shift keying.

Unit-V

(08 Hours)

Data Transmission:

Baseband signal receiver, probability of error, optimum filter, matched filter, probability of error of the matched filter, coherent reception. Detection of ASK, FSK & PSK signals through matched filter.

Unit-VI

(08 Hours)

Error, Control & Coding:

Parity, VRC, LRC, Linear block codes, CRC codes, Encoder/Decoder for block & CRC codes.

List of Practicals:

- To verify the sampling theorem & observe the aliasing effect.
- Study of Pulse Code modulation .
- Study of A law and μ -law companding techniques .
- To study Delta Modulation & Adaptive Delta Modulation
- To Study differential PCM.
- Study of code formats.
- Study of FSK & PSK.
- Study of QAM & QPSK.
- Study of Hamming code.
- Study of Cyclic code.

Text Books/References

- A.B. Carlson, "Communication Systems", McGraw Hill
- John Prokakis, "Digital Communication", PHI
- Taub & Schilling, "Principals of Communication System", McGraw Hill
- K. S. Shanmugan, "Digital & Analog Communication", PHI
- Simon Haykin, "Digital Communication", Wiley
- Wayhe Tomas l, "Communication Systems", PHI

- Leon W. Couch, "Digital & Analog Communication Systems", PEARSON Education Asia

Syllabus for Unit Test

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|-------------|---------------|
| Unit Test 1 | Unit I & II |
| Unit Test 2 | Unit III & IV |
| Unit Test 3 | Unit V & VI |



K50504: DISCRETE MATHEMATICS

TEACHING SCHEME

Lectures : 04 Hrs/week

EXAMINATION SCHEME

Theory : 70 Marks

Duration : 03 Hours

Unit Test : 30 Marks

Unit-I

(08 Hours)

Sets and Proposition & Computability and Formal Languages:

Introduction, Combinations of sets, Finite & Infinite Sets, Uncountably infinite sets. Mathematical induction. Principle of inclusion & exclusion. Russell's Paradox & Non-computability. Ordered sets. Languages. Phrase structure grammars.

Unit-II

(09 Hours)

Permutations, Combinations & Discrete Probability & Relations and Functions:

Introduction. The rules of sum & product. Permutations, combinations Discrete probability. A relational model for data bases. Properties of binary relations. Equivalence relations & partitions. Partial ordering relations & lattices. Chains & Antichains.

Unit-III

(07 Hours)

Graphs and Planar Graphs:

Introduction, Basic terminology, Multigraphs & weighted graphs, Paths & Circuits, Shortest path in weighted graphs.

Unit-IV

(07 Hours)

Trees and Cut-Sets:

Trees, Rooted trees. Path lengths in rooted trees. Prefix codes. Binary search trees.

Unit-V

(09 Hours)

Finite State Machines:

Introduction. Finite state machines. Finite state machines as models of physical systems. Equivalent machines.

Unit-VI

(08 Hours)

Analysis Of Algorithm:

Introduction, Time Complexity of Algorithm, A Shortest Path Algorithm, Complexity of Problems.

Text Books/References

- C.L.Liu, "Elements of Discrete Mathematics", 2nd Edition
- Marc Lipson, "Discrete Mathematics", 2nd Edition
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Syllabus for Unit Test

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|-------------|---------------|
| Unit Test 1 | Unit I & II |
| Unit Test 2 | Unit III & IV |
| Unit Test 3 | Unit V & VI |



SEMESTER - II





TEACHING SCHEME

Lectures : 04 Hrs/week

EXAMINATION SCHEME

Theory : 70 Marks

Duration : 03 Hours

Unit Test : 30 Marks

Unit-I

(08 Hours)

Linear Prediction and Optimum Filter Design :

Representation of stationary random process, Rational power spectra, Relationship between filter parameters and autocorrelation sequence, Forward and backward linear prediction, Solution of normal equations , properties of Lp error filters, AR Lattice and ARMA lattice ladder filters, Wiener filters, MA, AR, ARMA models, Least square filter design for prediction and deconvolution solution for least square estimation.

Unit-II

(08 Hours)

Adaptive Filters:

System identification, Adaptive channel equalization, Echo cancellation in data transmission over telephone channels, Suppression of narrowband interference in a wide band signal, Adaptive noise cancellation, LPC of speech signals, Adaptive direct form FIR filters, Adaptive lattice ladder filters, Design methods.

Unit-III

(08 Hours)

Power Spectrum Estimation :

Estimation of spectra from finite duration observations of signals, Non parametric methods for power spectrum estimation, Parametric methods, Minimum variance spectral estimation, Eigen analysis algorithms for spectrum estimation, Applications of DSP in speech and image processing.

Unit-IV

(08 Hours)

Introduction to Programmable DSPs:

DSP computational building blocks: Multiplier, MAC, Barrel shifter, ALU, Modified bus structure and memory access schemes in P-DSPs, Multiple

access memory, VLIW architecture, speed issues, addressing modes, features of external interfacing.

Unit-V

(08 Hours)

Development Tools for DSP Implementations:

Introduction, DSP Development tools, DSP system design kit, Software for development, Assembler and assembly source file, Linker and memory allocation, C/C++ compiler, CCS, DSP software development example.

Unit-VI

(08 Hours)

DSP Processor TMS320C6XXX:

Block diagram, Memory map, Peripheral registers, Signal groups, Device Configuration, Interrupts, Instruction set, Addressing modes and Interfacing.

Text Books/ References

- Proakis, "Advanced Digital Signal Processing", Prentice Hall International
- Oppenheim Schafer, "Discrete Time Signal Processing", Pearson education

Syllabus for Unit Test

| | |
|-------------|---------------|
| Unit Test 1 | Unit I & II |
| Unit Test 2 | Unit III & IV |
| Unit Test 3 | Unit V & VI |



TEACHING SCHEME

Lectures : 04 Hrs/week

EXAMINATION SCHEME

Theory : 70 Marks

Duration : 03 Hours

Unit Test : 30 Marks

Unit-I

(08 Hours)

Communication Concepts:

Circuit Designer Perspective, Modulation schemes, wireless channels, Path loss, Multipath fading.

Unit-II

(08 Hours)

Receiver Architecture:

Front end design, Filter design, Non linearity, Noise.

Unit-III

(08 Hours)

LNA & Mixer:

Wide band LNA design, Narrow band LNA, Impedance matching, Core amplifier.

Unit-IV

(08 Hours)

Analog to Digital Converter:

Demodulators, ADC's used in receiver, Low pass Sigma-Delta modulators, Band-pass Sigma-Delta modulators, Implementation of Sigma-Delta Modulators.

Unit-V

(08 Hours)

Frequency Synthesizer:

PLL based Frequency Synthesizer, Phase Detector, VCO, Oscillator: LC, Ring Oscillator.

Unit-VI

(08 Hours)

Loop Filter & System Design:

General description of loop filter, First, Second & Higher order filters, Loop filter design: Phase noise based approach & spur based approach, Complete synthesizer design.

Text Books/References

- Bosco Leung, "VLSI Design for Wireless Communication", Pearson Education

Syllabus for Unit Test

| | |
|-------------|---------------|
| Unit Test 1 | Unit I & II |
| Unit Test 2 | Unit III & IV |
| Unit Test 3 | Unit V & VI |





TEACHING SCHEME

Lectures : 04 Hrs/week
Practicals : 02 Hrs/week

EXAMINATION SCHEME

Theory : 70 Marks
Duration : 03 Hours
Unit Test : 30 Marks
Oral : 25 Marks
T.W. : 25 Marks

Unit-I

(08 Hours)

Hardware Design Concepts:

Arithmetic circuit designs, Circuit design for Boolean algebra implementation, Register Design of ACCUMULATOR of processors, Rotate and barrel shifting mechanism, Timers, counters and PWM Design.

Unit-II

(08 Hours)

Hardware Description Language:

Need for HDL, Basic Background and Concepts of HDLs, Correlation of HDL and Corresponding hardware generated.

Unit-III

(08 Hours)

Programmable Logic Devices:

Introduction to types of PLDs of various vendors(architecture and case study), JTAG Interface, IEEE and BSDL for ISP device programming, Various Modes of configuration.

Unit-IV

(08 Hours)

EDA Tool:

Design Flow, Synthesis Flow, Functional and Timing simulation and analysis, Physical Verification, Floor planning, place and route, IP Design.

Unit-V

(08 Hours)

Analog VLSI and High Speed VLSI:

Introduction to analog VLSI, Internal Architecture of FPAA, Implementation of designs on FPAA, Neural Networks and switched capacitor filters.

Unit-VI

(08 Hours)

Advanced VLSI Technology:

System on Chip, SoC and PSoC Architecture, Case study for Dynamic Reconfiguration, IRL: Internet Reconfigurable Logic, ILA: Internet Logic Analysis for testing the hardware within Chip, Testability Issues.

List of Practical

- Any eight assignments should be conducted based on above syllabus.
- Students should submit the record of these assignments as a term work.

Text Books/References

- Douglas A. Pucknell and Kamaran Eshraghian, "Basic VLSI Design Systems and Circuits", Prentice Hall of India Pvt. Ltd
- Wyane Wolf, "Modern VLSI Design", Prentice Hall
- Randall L. Geiger and P. E. Allen, "VLSI Design Techniques for Analog and Digital Circuits", McGraw Hill International Company
- Fabricious E., "Introduction to VLSI Design", McGraw Hill
- Peter J. Anderson, "The Designer's guide to VHDL", Harcourt Asia Private Limited & Morgan Kauffman
- John F. Wakerly, "Digital Design", Pearson Education 2002
- William I. Fletcher, "An Engineering Approach to Digital Design", Prentice Hall of India
- James E. Palmer, David E. Perlman, "Introduction to Digital Systems", Tata McGraw Hill
- N.N. Biswas, "Logic Design Theory", Prentice Hall of India
- S. Devadas, A. Ghosh and K. Keutzer, "Logic Synthesis", McGraw Hill

Syllabus for Unit Test

| | |
|-------------|---------------|
| Unit Test 1 | Unit I & II |
| Unit Test 2 | Unit III & IV |
| Unit Test 3 | Unit V & VI |



TEACHING SCHEME

Lectures : 04 Hrs/week

Practicals : 02 Hrs/week

EXAMINATION SCHEME

Theory : 70 Marks

Duration : 03 Hours

Unit Test : 30 Marks

Oral : 25 Marks

T.W. : 25 Marks

Unit-I

(08 Hours)

Introduction:

Simulation of pure-pursuit problem – an example, A system & its model, Simulation of an inventory problem, The basic nature of simulation, When to simulate.

Unit-II

(08 Hours)

Simulation of Continuous Systems:

A chemical reactor, Numerical integration vs. continuous system simulation, Selection of integration formula, Runge-Kutta integration formulae, Simulation of a servo system, Analog Vs Digital simulation.

Unit-III

(08 Hours)

Discrete System Simulation:

Fixed time-step vs. event to event model, On simulating randomness, Generation of random numbers, Generation of non-uniformly distributed random numbers, Monte-Carlo computation v/s stochastic simulation.

Unit-IV

(08 Hours)

Simulation of Queuing Systems:

Rudiments of queuing theory, Simulation of single server queue, Simulation of more general queues.

Unit-V

(08 Hours)

Simulation of A Pert Network:

Network model of a project, Analysis of an activity network, Critical path computation, Uncertainty in activity durations, simulation of activity network, Computer program for simulation, An example, Resource allocation and cost considerations..

Unit-VI

(07 Hours)

Simulation Experiments and Languages:

Length of simulation runs, Variance reduction techniques, Experimental Layout, Validation, Continuous and discrete simulation languages, Continuous simulation languages, Block-structured Continuous simulation languages, SIMSCRIPT, GPSS, SIMULA, Factors in selection of a discrete system simulation language.

List of Practical:

Any Ten experiments related with above topic.

Text Books/References

- Narsingh Deo, "System Simulation with Digital Computer", PHI Publication

Syllabus for Unit Test

| | |
|-------------|---------------|
| Unit Test 1 | Unit I & II |
| Unit Test 2 | Unit III & IV |
| Unit Test 3 | Unit V & VI |



SEMESTER - III



K50611 ELECTIVE I: TESTING OF VERIFICATION OF VLSI DESIGN

TEACHING SCHEME

Lectures : 04 Hrs/week

Practical : 02 Hrs/week

EXAMINATION SCHEME

Theory : 70 Marks

Duration : 03 Hours

Unit Test : 30 Marks

Termwork : 25 Marks

Oral : 25 Marks

Unit-I

(08 Hours)

Introduction :

Need for testing, the problems of digital & analog testing, design for test, Test economics and product quality, Fault modeling , Logic and fault simulation.

Faults in digital circuits: General introduction, controllability & observability, Fault models-Stuck at fault, bridging faults, intermittent faults.

Unit-II

(08 Hours)

Types of Tests:

Software testing, Testing sequential circuits, Random pattern testing, Memory testing, Analog & Mixed signal testing, Delay testing, VLSI testing process & test equipments.

Unit-III

(08 Hours)

Memory Tests:

Analog and mixed signal tests, Delay tests, IDDQ test.

Unit-IV

(08 Hours)

Testability Techniques:

Partitioning & adfoc methods & scan path testing, DFT techniques, BIST techniques, Boundary Scan Architecture & testing, ATPQ fundamental, Scan architecture & Techniques.

Unit-V

(08 Hours)

System Test:

Functional & Formal Verification's & Embedded core test , Future testing.

Unit-VI

(08 Hours)

VLSI Testing:

Digital tests pattern generation: test pattern generation for combinational logic circuits, manual test pattern generation, Automatic test pattern generation - Roth's D-algorithms, Developments following Roth's D algorithm, pseudorandom test pattern generation, test pattern generation for sequential circuits, Exhaustive, nonexhaustive & pseudorandom test pattern generation Delay fault testing.

Signatures & Self Test:

Input compression, output compression arithmetic & Red Muller coefficients, spectral coefficients, coefficient test signatures, signature analysis & online self test.

List of Practical

Minimum of one assignment on each topic should be conducted.

Text Books/ References

- Viswani D. Agrawal ,Michel L. Bushnell, "Essentials of Electronic Testing for Digital Memories & Mixed Signal VLSI Circuit", Kluwer Academic Publication
- Alfred L. Crouch, "Design for Test for Digital IC's & Embedded Core Systems" , PHI
- Stanley L. Hurst, "VLSI Testing: Digital & Mixed Analog Digital Techniques", Pub: Inspec/IEE.1999

Syllabus for Unit Test

| | |
|-------------|---------------|
| Unit Test 1 | Unit I & II |
| Unit Test 2 | Unit III & IV |
| Unit Test 3 | Unit V & VI |



K50611 ELECTIVE I: SOFTWARE DEFINED RADIOS

TEACHING SCHEME

Lectures : 04 Hrs/week

Practical : 02 Hrs/week

EXAMINATION SCHEME

Theory : 70 Marks

Duration : 03 Hours

Unit Test : 30 Marks

Termwork : 25 Marks

Oral : 25 Marks

Unit-I

(08 Hours)

Introduction to Software Radio Concepts:

Need for Software Radios, Characteristics , benefits & design principles of Software radios.

Unit-II

(08 Hours)

Radio Frequency Implementation Issues:

Purpose of RF front end, Dynamic range: Principal challenge of receiver design, RF receiver front end topologies, Importance of components to overall performance, Transmitter architecture & their issues, Noise & distortion in RF chain, ADC & DAC distortion.

Unit-III

(08 Hours)

AD/DA Converters for Software Radios:

Parameters of ideal data converters, Parameters of practical data converters, Data converters, Data converter performance improvement techniques, common ADC & DAC architectures.

Unit-IV

(08 Hours)

Smart Antennas :

Benefits of Smart Antennas, Structures for Beamforming Systems, Smart Antenna Algorithms, Diversity & space-Time Adaptive signal processing, Algorithms for transmit STAP, Hardware implementation of smart antenna, Array calibration.

Unit-V

(08 Hours)

Digital Hardware Choices:

Key Hardware elements, DSP Processors, FPGAs, Tradeoffs in using DSPs, FPGAs, & ASICs Power management issues.

Unit-VI

(08 Hours)

Case Studies in Software Radio:

SPEAKEasy, JTRS.

List of Practical

- MATLAB simulation of a Wireless Communication Systems .
- Design & Develop simulink model for ADC & DAC .
- Study of ADC/DAC distortion .
- Study of smart Antennas.
- Design of simulate MIMO system.
- Implementation of communication system on DSP.
- Implementation of ADC - DAC on VLSI kit.
- Implementation of SDR communication system

Text Books/References

- J. H. Reed, "Software Radio: A Modern Approach to Engineering", Pearson Education, First Edition, 2002

Syllabus for Unit Test

| | |
|-------------|---------------|
| Unit Test 1 | Unit I & II |
| Unit Test 2 | Unit III & IV |
| Unit Test 3 | Unit V & VI |



K50611 ELECTIVE I: REAL TIME SYSTEM DESIGN

TEACHING SCHEME

Lectures : 04 Hrs/week

Practical : 02 Hrs/week

EXAMINATION SCHEME

Theory : 70 Marks

Duration : 03 Hours

Unit Test : 30 Marks

Termwork : 25 Marks

Oral : 25 Marks

Unit-I

(08 Hours)

Basics Real-time concepts:

Architecture, Design Issues, CPU: Addressing Modes, Interrupts, RISC Machines, Memories, Input-Output Devices.

Unit-II

(08 Hours)

Language & Software Lifecycle:

Language Features, Code generation, Scheduleability analysis, Phases of software lifecycles, Non-temporal transitions in the software life cycle, Spiral model, other Standards.

Unit-III

(08 Hours)

Real-time specification & Design Techniques:

Mathematical specifications, Dataflow diagram, Petri Nets, warnier-Orr Natation , State charts, Real-time kernels, Polled loop systems, Phase/State driven Code, Coroutinnes, Interrupt-driven systems. RTOS.

Unit-IV

(08 Hours)

Real-time Memory Management:

Buffering data, Mailboxes, Semaphores, Events flags & Signals, Deadlock, Process Stack management, Dynamic allocation.

Unit-V

(08 Hours)

System Performance Analysis & Optimization:

Response time calculation, Interrupt latency, time loading & Its measurements, Scheduling, Reducing response time & time loading & its

measurements, Scheduling, Reducing response time & time loading, Analysis of memory requirements, reducing memory loading.

Unit-VI

(08 Hours)

Reliability testing & Fault Tolerance:

Faults, failures, bugs & effects, reliability, testing, fault tolerance, Goals of real-time system integration Methodology, Real-time applications, Image Processing, Unix.

List of Practical

Minimum of one assignment on each topic should be conducted.

Text Books/References

- Phillip A. Laplante, "Real-Time Systems Design & Analysis", PHI Publication-Second Edition

Syllabus for Unit Test

| | |
|-------------|---------------|
| Unit Test 1 | Unit I & II |
| Unit Test 2 | Unit III & IV |
| Unit Test 3 | Unit V & VI |



K50612 ELECTIVE II: WIRELESS SENSORS NETWORKS

TEACHING SCHEME

Lectures : 04 Hrs/week

Practical : 02 Hrs/week

EXAMINATION SCHEME

Theory : 70 Marks

Duration : 03 Hours

Unit Test : 30 Marks

Termwork : 25 Marks

Oral : 25 Marks

Unit-I

(08 Hours)

Introduction:

Unique Constraints & challenges, Advantages of sensor networks, Sensor network Application, Collaborative processing, Key definitions of sensor networks.

Unit-II

(08 Hours)

Localization & Tracking:

A tracking scenario, problem formulation, Distributed Representation & interface of states, Tracking multiple objects, Sensor models, Performance Comparison & metrics.

Unit-III

(08 Hours)

Networking Sensors:

Key Assumptions, Medium Access Control, General issues, Geographic & Energy-Aware Routing, Attribute-Based Routing.

Unit-IV

(08 Hours)

Infrastructure Establishment:

Topology control, Clustering, Time Synchronization, Localization & Localization Services.

Unit-V

(08 Hours)

Sensor Tasking Control:

Task-Driven Sensing, Roles of sensor nodes & utilities, information-based sensor tasking, Joint Routing & information Aggregation.

Unit-VI

(08 Hours)

Sensor Network Platforms & Tools:

sensor node hardware, Sensor network, Programming Challenges, Node-Level software platforms, Node-level Simulators.

List of Practical

Minimum of one assignment on each topic should be conducted.

Text Books/References

- Feng Zhao, Leonidas J. Guibas, Elsevier, "Wireless Sensor Networks: An Information Processing Approach", First edition, 2006

Syllabus for Unit Test

| | |
|-------------|---------------|
| Unit Test 1 | Unit I & II |
| Unit Test 2 | Unit III & IV |
| Unit Test 3 | Unit V & VI |



K50612 ELECTIVE II: ALGORITHM FOR VLSI DESIGN AUTOMATION

TEACHING SCHEME

Lectures : 04 Hrs/week

Practical : 02 Hrs/week

EXAMINATION SCHEME

Theory : 70 Marks

Duration : 03 Hours

Unit Test : 30 Marks

Termwork : 25 Marks

Oral : 25 Marks

Unit-I

(08 Hours)

Logic Synthesis & Verification:

Introduction to combinational logic synthesis, binary decision diagram, Hardware models for high-level synthesis.

Unit-II

(08 Hours)

Partitioning:

Problem formulation, Classification of partitioning algorithms, Group migration algorithms, simulated annealing & evolution, other partitioning algorithms.

Unit-III

(08 Hours)

Placement, Floor Planning & Pin Assignment:

Problem formulation, Simulation based placement algorithms, other placement algorithms, Constrain based floor planning, floor planning algorithms for mixed block & cell design, General & channel pin assignment.

Unit-IV

(08 Hours)

Global Routing:

Problem formulation, classification of global routing algorithms, Maze routing algorithms, Line probe algorithm, Steiner tree based algorithms, ILP based approaches.

Unit-V

(08 Hours)

Detailed Routing:

Problem formulation, classification of routing algorithms, single layer

routing algorithms, Two layer channel routing algorithm, Three layer channel routing algorithm & switch box routing algorithms.

Unit-VI

(08 Hours)

Over The Cell Routing & Via Minimization:

Two layers over the cell routers, Constrained & unconstrained via minimization.

Compaction:

Problem formulation, one-dimensional compaction, Two dimension based compaction, hierarchical compaction.

List of Practical

Minimum one assignment on each topic should be conducted.

Text Books/ References

- Christophn Meinel & Thorsten Thcobold, "Algorithms & Data Structures for VLSI Design", KAP, 2002
- Rolf Drecshseler, "Evolutionary Algorithms for VLSI", 2nd edition
- Trimburger, "Introduction to CAD for VLSI", Kluwer Academic Pub, 2002
- Naveed Shervani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Pub, 2nd edition

Syllabus for Unit Test

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|-------------|---------------|
| Unit Test 1 | Unit I & II |
| Unit Test 2 | Unit III & IV |
| Unit Test 3 | Unit V & VI |



K50612 ELECTIVE II: FUZZY LOGIC FOR EMBEDDED SYSTEM APPLICATION

TEACHING SCHEME

Lectures : 04 Hrs/week

Practical : 02 Hrs/week

EXAMINATION SCHEME

Theory : 70 Marks

Duration : 03 Hours

Unit Test : 30 Marks

Termwork : 25 Marks

Oral : 25 Marks

Unit-I

(08 Hours)

Fuzzy Sets:

Basic components of fuzzy sets, Determination of membership functions, fuzzy set properties, operations on fuzzy sets.

Unit-II

(08 Hours)

Fuzzy Relations:

Classical relations, Fundamentals of fuzzy relations, Operations on binary fuzzy relations, types of fuzzy relations, fuzzy reasoning.

Unit-III

(08 Hours)

Embedded Fuzzy Applications:

Conventional control systems- Description, analysis & design, PID control, Fuzzy logic controller-Description, design, defuzzification & analysis, Applications: Washing machine, Vacuum cleaner.

Unit-IV

(08 Hours)

Neural Networks:

Basic neuron model, perceptron, multilayer perceptron, Hopfield networks, Boltzman machine networks, Kohonen self organizing networks, adaptive resonance theory.

Unit-V

(08 Hours)

Hybrid Systems:

Fuzzy-neuron, multilayer FNN architectures, Fuzzy ART, Fuzzy ART MAP, Neural- Fuzzy Systems.

Unit-VI

(08 Hours)

Hardware Implementations:

Digital Techniques, Analog Techniques. Fuzzy analog memory, neurons.

List of Practical

- Assignment on fuzzy sets.
- Assignment on fuzzy operation.
- Simulink simulation of fuzzy controller.
- Simulink model for washing machine.
- Simulink model for vacuum cleaner.
- Two assignments on neural networks.
- Design of Neural network using matlab.

Text Books/References

- A. M. Ibrahim, Elsevier, "Fuzzy Logic for Embedded System Applications", 1st Edition, 2004

Syllabus for Unit Test

| | |
|-------------|---------------|
| Unit Test 1 | Unit I & II |
| Unit Test 2 | Unit III & IV |
| Unit Test 3 | Unit V & VI |



RULES REGARDING ATKT, CONTINUOUS ASSESSMENT AND AWARD OF CLASS

A. T. K. T.

- A candidate who is granted term for B.Tech. Semester-I will be allowed to keep term for his/her B.Tech. Semester-II examination even if he/she appears and fails or does not appear at B.Tech. Semester-I examination.
- A candidate who is granted term for B. Tech. Semester - III will be allowed to keep term for his/her B.Tech. Semester-IV examination even if he/she appears and fails or does not appear at B.Tech. Semester-III examination.
- A candidate who is granted term for B.Tech. Semester-V will be allowed to keep term for his/her B.Tech. Semester-VI examination if he/she appear and fails or does not appear at B.Tech. Semester-V examination.
- A candidate who is granted term for B.Tech. Semester-VII will be allowed to keep term for his/her B.Tech. Semester-VIII examination if he/she appears and fails or does not appear at B.Tech. Semester-VII examination.
- A student shall be allowed to keep term for the B.Tech. Semester-III course if he/she has a backlog of not more than 3 Heads of passing out of total number of Heads of passing in theory examination at B.Tch. Semester-I & II taken together.
- A student shall be allowed to keep term for the B.Tech. Semester-V of respective course if he/she has no backlog of B.Tech Semester-I & II and he/she has a backlog of not more than 3 Heads of passing in theory examination and not more than 3 heads of passing in termwork and practical examination or termwork and oral examination.
- A student shall be allowed to keep term for the B.Tech. Semester-VII course if he/she has no backlog of B.Tech. Semester-III & IV and he/she has a backlog of not more than 3 Heads of passing in theory examination and not more than 3 Heads of passing in termwork and practical examination or termwork and oral examination.

CONTINUOUS ASSESSMENT

- In respect of Term work at B.Tech. Semester-I & II, B.Tech. Semester-III & IV and B.Tech. Semester-V & VI, target date shall be fixed for the completion of each job, project experiment or assignment as prescribed in the syllabus and the same shall be collected on the target date and assessed immediately at an affiliated college by at least one pair of the concerned teachers for the subject and the marks shall be submitted at the end of each term to the Principal of the college.

- Termwork and performance of Practical/Oral examination shall be assessed on the basis of the depth of understanding of the principles involved, correctness of results and not on ornamental or colorful presentation.
- For B.Tech. Semester-VII & VIII, termwork assessment will be done by external and internal examiners jointly during the examination schedule declared by the university. The record of continuous assessment shall be made available to the examiners during Term work and practical and Term work and oral examinations. Examiner shall use this record for overall assessment of the performance of the student. Every practical/termwork assignment shall be assessed on the scale of 20 marks and weightage of 20 marks shall be distributed as follows:

| Sr. No. | Activity | Marks |
|---------|-------------------|-------|
| 1 | Timely Submission | 04 |
| 2 | Presentation | 06 |
| 3 | Understanding | 10 |

Marks obtained out of 20 for all assignments together will be converted on scale of marks assigned to term work of respective subject in the structure of the course.

CLASS

- The class should be awarded to the student on the basis of aggregate marks obtained together in both the semesters of the respective year by him. The award of class shall be as follows.

| | | |
|---|---|------------------------------|
| A | Aggregate 66% or more marks | First Class with Distinction |
| B | Aggregate 60% or marks but less than 66% | First Class |
| C | Aggregate 55% or more marks but less than 60% | Higher Second Class |
| D | Aggregate 50% or more marks but less than 55% | Second Class |
| E | Aggregate 40% or more marks but less than 50% | Pass Class |